IN THE CLAIMS

Following are the current claims. For the claims that have **NOT** been amended in this response, any differences in the claims below and the current state of the claims is unintentional and in the nature of a typographical error.

1. (Previously Presented) A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;

a data cache capable of storing data values used by said pending instruction;

a plurality of registers capable of receiving said data values from said data cache;

a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;

a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, or c) zero extending said first data value prior to loading said first data value into said target register; and

bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

2. (Original) The data processor as set forth in Claim 1 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation.

3. (Original) The data processor as set forth in Claim 2 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register at the end of two machine cycles.

4. (Previously Presented) The data processor as set forth in Claim 1 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation.

5. (Original) The data processor as set forth in Claim 4 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

6. (Previously Presented) The data processor as set forth in Claim 1 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation.

7. (Original) The data processor as set forth in Claim 6 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

8. (Original) The data processor as set forth in Claim 1 wherein said bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache.

9. (Original) The data processor as set forth in Claim 8 wherein said multiplexer has a second input channel coupled to an output of said shifter circuit.

10. (Previously Presented) A method of loading a first data value from a data cache into a target register of a plurality of registers, the method comprising the steps of:

determining if a pending instruction in an N-stage execution pipeline is one of a load word operation, a load half-word operation, and a load byte operation;

in response to a determination that the pending instruction is a load half-word operation, transferring the first data value from the data cache to a shifter circuit and shifting the first data value prior to loading the first data value into the target register;

in response to a determination that the pending instruction is a load byte operation, transferring the first data value from the data cache to the shifter circuit and shifting the first data value prior to loading the first data value into the target register; and

in response to a determination that the pending instruction is a load word operation, transferring the first data value from the data cache directly to the target register without processing the first data value in the shifter circuit.

11. (Original) The method as set forth in Claim 10 wherein the step of transferring the first data value requires two machine cycles during a load word operation.

12. (Original) The method as set forth in Claim 10 wherein the step of transferring the first data value requires three machine cycles during a load half-word operation.

13. (Original) The method as set forth in Claim 10 wherein the step of transferring the first data value requires three machine cycles during a load byte operation.

14. (Previously Presented) A processing system comprising:

a data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;

a data cache capable of storing data values used by said pending instruction;

a plurality of registers capable of receiving said data values from said data cache;

a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;

a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, or c) zero extending said first data value prior to loading said first data value into said target register; and

bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit;

a memory coupled to said data processor; and

a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor.

15. (Original) The processing system as set forth in Claim 14 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation.

16. (Original) The processing system as set forth in Claim 15 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register at the end of two machine cycles.

17. (Previously Presented) The processing system as set forth in Claim 14 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation.

18. (Original) The processing system as set forth in Claim 17 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

19. (Previously Presented) The processing system as set forth in Claim 14 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation.

20. (Original) The processing system as set forth in Claim 19 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

21. (Original) The processing system as set forth in Claim 14 wherein said bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache.

22. (Original) The processing system as set forth in Claim 21 wherein said multiplexer has a second input channel coupled to an output of said shifter circuit.

23. (New) A processor, comprising:

a cache;

a plurality of registers;

a shifter circuit capable of shifting, sign extending, or zero extending a data value from the cache and providing a modified data value to a target one of the registers; and

a bypass circuit capable of transferring the data value from the cache to the target register without processing the data value in the shifter circuit.

24. (New) The processor of Claim 23, wherein:

the data value is transferred from the cache to the target register via the bypass circuit during a load word operation; and

the data value is transferred from the cache to the target register via the shifter circuit during a load half-word operation or a load byte operation.

25. (New) The processor of Claim 24, wherein:

the bypass circuit is capable of transferring the data value from the cache to the target register at an end of two machine cycles; and

the shifter circuit is capable of providing the modified data value to the target register at an end of three machine cycles.

26. (New) The processor of Claim 23, wherein the bypass circuit comprises a multiplexer having a first input coupled to the cache and a second input coupled to the shifter circuit.

27. (New) A method, comprising:

shifting, sign extending, or zero extending a first data value from a cache and providing a modified first data value to a first of a plurality of registers; and

transferring a second data value from the cache to a second of the plurality of registers without shifting, sign extending, or zero extending the second data value.

28. (New) The method of Claim 27, wherein:

shifting, sign extending, or zero extending the first data value comprises shifting, sign extending, or zero extending the first data value in response to determining that a first pending instruction in a processor is a load byte operation or a load half-word operation; and

transferring the second data value comprises transferring the second data value to the second register in response to determining that a second pending instruction in the processor is a load word operation.

29. (Previously Presented) A system, comprising:

a processor comprising:

a cache;

a plurality of registers;

a shifter circuit capable of shifting, sign extending, or zero extending a data value from the cache and providing a modified data value to a target one of the registers; and

a bypass circuit capable of transferring the data value from the cache to the target register without processing the data value in the shifter circuit;

a memory coupled to the processor; and

a plurality of peripheral circuits capable of performing selected functions in association with the processor.